CLAIMS

What is claimed is:

1. A semiconductor device comprising:

a plurality of flash memory cells, wherein said cells have more than two storage conditions; and

wherein said cells are programmable from a first non-erased state directly to a second programmed state.

2. The semiconductor device as described in Claim 1 further comprising a page buffer, wherein said page buffer is for combining existing cell storage conditions with new partial page information.

3. The semiconductor device as described in Claim 2 wherein said page buffer comprises pre-charged registers.

4. The semiconductor device as described in Claim 2 further comprising logic to combine said existing cell storage conditions with said new partial page information.

5. The semiconductor device as described in Claim 4 wherein said logic is operable to produce allowable partial page program transitions.

6. A method of programming a partial page in a multi level flash device comprising:

a) presenting new programming information to said device; and

b) programming said new information in said device, without an interposing erase operation.

7. The method as described in Claim 6 further comprising:

a1) reading existing cell storage conditions from said device.

8. The method as described in Claim 6 wherein said reading is automatically performed internally to said device.

9. The method as described in Claim 6 wherein said existing cell storage conditions are copied into a page buffer.

10. The method as described in Claim 6 further comprising:

a2) combining said existing cell storage conditions with programming information to produce new information.

11. The method as described in Claim 10 further wherein said combining is automatically performed internally to said device.

12. The method as described in Claim 10 wherein said combining is performed in memory external to said device.

13. The method as described in Claim 10 further wherein said combining takes place in a page buffer.

14. A semiconductor device comprising:

a plurality of flash memory cells, wherein said cells have more than two storage conditions; and

wherein said cells are programmable from a first non-erased state to a second programmed state without an interposing erase operation.

15. The semiconductor device as described in Claim 14 further comprising a page buffer, wherein said page buffer is for combining existing cell storage conditions with new partial page information.

16. The semiconductor device as described in Claim 14 further comprising logic to combine said existing cell storage conditions with said new partial page information.

17. The semiconductor device as described in Claim 16 wherein said logic is operable to produce allowable partial page program transitions.

18. A semi conductor device comprising:

a bus;

a plurality of external ports for receiving programming information coupled to said bus;

a plurality of memory cells, for the non-volatile storing of information, wherein said memory cells have more than two storage states coupled to said bus;

a page buffer, for combining new programming information with previously stored information to produce program verify information, wherein said page buffer is composed of pre-charged registers coupled to said bus; and

a state machine for placing new said programming information into said page buffer coupled to said bus;

said state machine also for placing previously stored information into said page buffer;

said state machine also for programming said program verify information into said memory cells.

19. A computer system comprising:

a processor coupled to a bus;

a first multi level cell flash memory coupled to said bus; and

wherein said computer system contains instructions which when implemented perform a method of programming a partial page in said first multi level cell flash memory, said method comprising:

a) presenting new programming information to said first multi level cell flash memory; and

b) programming said new information in said first multi level cell flash memory, without an interposing erase operation.

20. The method as described in Claim 19 further comprising:

a1) reading existing cell storage conditions from said device.

21. The method as described in Claim 20 wherein said reading is automatically performed internally to said device.

22. The method as described in Claim 20 wherein said existing cell storage conditions are copied into a page buffer.

23. The method as described in Claim 20 further comprising:

a2) combining said existing cell storage conditions with programming information to produce new information.

24. The method as described in Claim 23 further wherein said combining is automatically performed internally to said first multi level cell flash memory.

25. The method as described in Claim 22 wherein said computer system further comprises a second memory connected to said bus, and wherein said combining is performed in said second memory.